CLAIMS

What is claimed is:

1. A debugging system, comprising:

a processor constructed to execute a software process;

a fast-response circuit coupled to a low-level asset in the processor;

the fast response circuit configurable to extract selectively data from the low-level asset; and

a data path extending from the fast response circuit and constructed to transmit extracted evidence data to an evidence file.

2. A debugging system, comprising:

a processor constructed to execute a software process;

a fast-response circuit coupled to a low-level asset in the processor;

the fast response circuit configurable to monitor selectively data from the low level asset for a predetermined event; and

an action line extending from the fast response circuit and constructed to transmit an action signal responsive to the event.

3. A debugging system, comprising:

a processor constructed to execute a software process;

a fast-response circuit coupled to a low-level data asset in the processor;

the fast response circuit having a first portion configurable to monitor data from the low level asset for a predetermined event, and constructed to generate an action signal upon the occurrence of the predetermined event;

the fast response circuit having a second portion configurable to extract selectively data from the low-level asset, and constructed to act responsive to the action signal; and

a data path extending from the fast response circuit and constructed to transmit extracted evidence data to an evidence file.

4. The debugging system of claim 1, 2, or 3, wherein the low-level asset is constructed as a commit buffer, a reorder buffer, a high speed data bus, or a register.

5. The debugging system of claim 1, 2, or 3 wherein the fast response circuit is integrated on-chip with the low-level asset of the processor.

6. The debugging system of claim 1, 2, or 3, wherein the fast response circuit comprises high speed registers.

7. The debugging system of claim 1, 2, or 3, wherein the data path is a high speed bus extending from the fast response circuit to a cache on-chip with the processor.

8. The debugging system according to claim 3, further including:

sequential logic connected to the first portion of the fast response circuit; and

wherein the sequential logic is programmable to selectively monitor for compound process events, and the sequential logic enables an action responsive to the compound process events.

9. The debugging system according to claim 3, further including:

sequential logic connected to the second portion of the fast response circuit; and

wherein the sequential logic is programmable to selectively extract data according to compound criteria.

10. The debugging system according to claim 8 or 9, wherein the sequential logic is constructed as a co-processor.

11. The debugging system according to claim 8 or 9, wherein the sequential logic is integrated on-chip with the low-level asset of the processor.

12. A processor chip, comprising:

a low-level asset;

a fast-response circuit coupled to the low-level asset;

the fast response circuit having a first portion configurable to monitor data from the low level asset for a predetermined event, and constructed to generate an action signal upon the occurrence of the predetermined event;

the fast response circuit having a second portion configurable to extract selectively data from the low-level asset, and constructed to act responsive to the action signal; and

a data path extending from the fast response circuit to a cache memory, the data path constructed to transmit extracted evidence data to an evidence file.

13. An evidence file in computer readable format, comprising data selectively extracted from a low-level asset in a central processing unit.

14. A processor comprising:

a low level asset;

a fast response circuit;

a high-speed data path constructed to transmit data from the low level asset to the fast response circuit;

wherein the processor performs the steps of:

pre-configuring the fast response logic to monitor for an event

pre-configuring the fast response logic to extract data selectively;

executing a central-program;

detecting the event using the fast response logic;

extracting data selectively using the fast response logic; and

transferring the extracted data to a cache memory.

15. The processor according to claim 14, further comprising:

a second low-level asset connected to the fast response circuit; and

wherein the extracting step includes selectively extracting data from the second low-level asset.

16. The processor according to claim 14, further comprising:

a sequential logic circuit connected to the fast response circuit; and

wherein the processor performs the steps of:

transmitting an action signal to the sequential logic responsive to detecting the event.

17. An automated method of examining an evidence file, the method using a computing system, comprising:

providing an evidence file, the evidence file having data collected from a processing unit;

identifying that a branch instruction has failed to execute as expected;

setting a search definition intended to locate the branch instruction;

searching for a data portion in the evidence file that is indicative that the branch instruction was available for the processing unit to execute;

detecting, using the data portion, the that branch instruction was not executed when available; and

examining the data portion.

18. An method of generating an evidence file from a processor, comprising:

identifying that a branch instruction has failed to execute as expected in a software program;

setting a search definition intended to locate the branch instruction;

monitoring data from the processor to find a data portion that is indicative that the branch instruction was available for the processing unit to execute;

detecting, using the data portion, the that branch instruction was not executed when available; and

extracting the data portion to an evidence file.